WHAT IS CLAIMED IS:

1. A landing pad for use as a contact to a conductive spacer adjacent a structure in a semiconductor device, said landing pad comprising:

two islands, each substantially rectangularly shaped and spaced apart from one another and from the structure; and

conductive spacers adjacent to each island and overlapping each other and overlapping with the conductive spacer adjacent to the structure;

wherein contact to the landing pad is on the conductive spacers adjacent to the islands and spaced apart from the structure.

2. The landing pad of claim 1 wherein said conductive spacers are made of conductive polysilicon.

3. The landing pad of claim 2 wherein the islands are spaced apart form one another by a distance which is less than twice the width of each conductive spacer.

4. The landing pad of claim 3 wherein the islands are spaced apart from the structure by a distance which is less than twice the width of each conductive spacer.

5. A method of forming a landing pad to a conductive spacer adjacent a structure, said method comprising:

forming the structure on a semiconductor substrate, said structure having a substantially planar side;

forming two islands on the semiconductor substrate, each island substantially rectangularly shaped and spaced apart from one another and from the planar side of the structure;

forming conductive spacers adjacent to the planar side of the structure between the structure and the islands, and adjacent to each of the islands, surrounding each island, with said conductive spacers overlapping one another between the islands and between the islands and the structure; and

forming a landing pad, said landing pad being on said conductive spacers, between the islands and between the islands and the structure.

6. The method of claim 5 wherein said conductive spacers are made of conductive polysilicon.

7. The method of claim 6 wherein said forming conductive spacers step further comprises:

conformally depositing a layer of polysilicon on said islands and on said structure and therebetween;

anisotropically etching said layer of polysilicon to form said conductive spacers.

8. The method of claim 7 wherein said forming a landing step further comprises:

masking said islands, structure and conductive spacers with a layer of insulating material;

selectively removing a portion of said layer of insulating material at a position between the islands and between the islands and the structure to form the landing pad.

9. The method of claim 8 wherein the islands are spaced apart form one another by a distance which is less than twice the width of each conductive spacer.

10. The method of claim 9 wherein the islands are spaced apart from the structure by a distance which is less than twice the width of each conductive spacer.

11. A non-volatile memory device comprising:

an array of non-volatile memory cells arranged in a plurality of rows and columns wherein cells in the same row are connected by a common spacer shaped control gate adjacent a structure;

a plurality of spaced apart landing pads adjacent each control gate, each landing pad comprising two substantially rectangularly shaped spaced apart islands, each having a spacer adjacent to the island, wherein the spacer adjacent to one island overlaps the spacer adjacent the other island, and wherein the spacers of the islands overlap the adjacent common spacer shaped control gate;

a layer of insulating material covering the spacers of the islands, the common spacer shaped control gate and the islands, with the insulating material having a hole through the insulating material, said hole positioned between the islands and between the islands and the structure;

a conductive layer on the layer of insulating material connecting through the hole to the control gate.

12. The memory device of claim 11 wherein the common spacer shaped control gate is made of conductive polysilicon.

13. The memory device of claim 12 wherein the spacers adjacent to the islands are made of conductive polysilicon.

14. The memory device of claim 13 wherein the structure comprises:

a floating gate insulated from the control gate by a tunneling material; said floating gate having a tip for facilitating the tunneling of charges from the floating gate through the tunneling material to the control gate.

15. The memory device of claim 14 wherein the array comprises a plurality of spaced apart control gates, each gate extending in the row direction and wherein the distance of separation between each adjacent control gate is greater at the location with the landing pad therebetween than at the location without the landing pad.

16. The memory device of claim 15 wherein an isolation region separates each column of cells.

17. A method of detecting one or more defects in a string of spaced apart studs on a semiconductor substrate wherein each stud is separated by a distance of 2X from an adjacent stud, said method comprising:

forming a plurality of conductive spacers with each spacer formed adjacent each stud, and overlapping with an adjacent spacer, each spacer having a width of at least X; and

electrically testing the continuity of the plurality of conductive spacers;

wherein in the event of failure of the testing step, said failure is indicative of the existence of one or more defects.

18. The method of claim 17 wherein said step of forming a plurality of conductive spacers comprises:

depositing conformally a layer of conductive polysilicon over said string of studs;

anisotropically etching said layer of conductive polysilicon to form said plurality of conductive spacers.

19. A method of detecting one or more defects in a string of spaced apart holes in a semiconductor device wherein each hole is separated by a distance of 2X from an adjacent hole, said method comprising:

converting each hole into a stud;

forming a plurality of conductive spacers with each spacer formed adjacent each stud, and overlapping with an adjacent spacer, each spacer having a width of at least X; and

electrically testing the continuity of the plurality of conductive spacers;

wherein in the event of failure of the testing step, said failure is indicative of the existence of one or more defects.

20. The method of claim 19 wherein said step of forming a plurality of conductive spacers comprises:

depositing conformally a layer of conductive polysilicon over said string of studs;

anisotropically etching said layer of conductive polysilicon to form said plurality of conductive spacers.

21. The method of claim 19 wherein said converting step comprises a damascene process.